REMARKS

The present *Supplemental Amendment* supplements the *Amendment* filed on August 9, 2006, and is submitted further in response to the Official Action dated February 9, 2006.

The Applicant appreciates Examiner Duong's time in conducting a personal interview on November 9, 2006. As described in more detail below, during the interview the Applicant's representative explained that the capacitive wiring of the present claims differs from gate wiring. Agreement was reached to amend the claims to recite "capacitive wiring" instead of "wiring." Also, per the Examiner's request, the Applicant provides more details as to the support for the new claims. The Examiner agreed to consider the Applicant's remarks following the submission of this *Supplemental Amendment*.

Claims 1, 3, 5 and 50-120 are pending in the present application, of which claims 1, 5 and 50-83 are independent. Independent claims 1 and 50-77 and dependent claims 3 and 89-91 have been amended to better recite the features of the present invention. The Applicant notes with appreciation the allowance of claim 5 (telephonic interview conducted the week of May 1, 2006; per agreement, summarized in the *Amendment* filed August 9, 2006). For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

As noted in detail in the *Response* filed August 9, 2006, the only remaining rejections from the Official Action dated February 9, 2006, are as follows: The Official Action rejects claims 1 and 3 under the doctrine of obviousness-type double patenting over the claims of U.S. Patent No. 6,693,681 to Takemura. With respect to claims 1 and 3, the Applicant respectfully submits that amended independent claim 1 of the subject application is patentably distinct from the claims of the Takemura patent and Tsukada.

As stated in MPEP § 804, under the heading "Obviousness-Type," in order to form an obviousness-type double patenting rejection, a claim in the present application

must define an invention that is merely an obvious variation of an invention claimed in the prior art patent, and the claimed subject matter must not be patentably distinct from the subject matter claimed in a commonly owned patent. Also, the patent principally underlying the double patenting rejection is not considered prior art.

The Applicant respectfully traverses the obviousness-type double patenting rejection. Independent claim 1 of the present application has been amended to recite an insulating flattening film over a capacitive wiring and a reverse stagger type amorphous silicon thin film transistor, which is supported in the present specification, for example, by Figures 1(A) and 5; and page 14, lines 16-20, which discloses the following:

> Fig. 5 shows an embodiment of a method of forming the TFT and the picture element as described above. In this embodiment, a reverse stagger type which is used for amorphous silicon TFT is formed. However, the same back-surface exposure technique can be used for a planar type.

The claims of Takemura and Tsukada do not teach or suggest the above-referenced features. It is respectfully submitted that the claims of the present application are not a timewise extension of the invention as claimed in the Takemura patent, either alone or in combination with Tsukada. Reconsideration and withdrawal of the obviousness-type double patenting rejections are requested.

New claims 50-120 have been added to recite additional protection to which the Applicant is entitled.

New independent claim 50 further limits claim 1 in that claim 50 recites that a sum of a capacitance between the transparent pixel electrode and the gate line and the capacitance between the transparent pixel electrode and the capacitive wiring is above ten times as large as a difference between the capacitance between the transparent pixel electrode and the gate line and the capacitance between the transparent pixel electrode and the capacitive wiring. This feature is supported in the present specification, for example, at page 7, lines 8-13, which discloses that a sum of a capacitance between the transparent pixel electrode and the gate line and the

capacitance between the transparent pixel electrode and the wiring is above ten times as large as a difference between the capacitance between the transparent pixel electrode and the gate line and the capacitance between the transparent pixel electrode and the wiring. Specifically, for example, the present specification discloses the following:

> If this invention is applied to obtain the same effect, the sum of C_1 and C_2 (parasitic capacitance of TFT is contained in C_1 and C_2) is required to be set to a value above ten times as large as the difference between C_1 and C_2, and this requirement can be relatively easily achieved.

New independent claim 51 further limits claim 1 in that claim 51 recites that a capacitance induced by an overlap between the data line and the transparent pixel electrode is smaller than the capacitances between the transparent pixel electrode and the gate line and the transparent pixel electrode and the capacitive wiring. This feature is supported in the present specification, for example, by the first full paragraph of page 13, which discloses that a capacitance induced by an overlap between the data line and the transparent pixel electrode is smaller than the capacitances between the transparent pixel electrode and the gate line and the transparent pixel electrode and the wiring. Specifically, for example, the present specification discloses the following:

> No problem arises in the overlap between the data lines and the picture-element electrodes. Of course, signals of the data lines flow into the picture element concerned, and they act as noises, so that a phenomenon such as a so-called cross-talk may occur. However, the degree of this phenomenon can be sufficiently suppressed. For example, the interval of the gate lines may be narrowed so that the capacitance induced by the overlap between the data line and the pixel electrode (picture-element electrode) is reduced to a value smaller than the auxillary capacitances C_1 and C_2 (the capacitances of the capacitors formed by the pixel electrode and the gate lines).

New independent claim 52 is a combination of claims 50 and 51.

New independent claim 53 further limits claim 1 in that claim 53 recites that when a first pulse is applied to the gate line, a second pulse having an opposite polarity to the first pulse is applied to the capacitive wiring. This feature is supported in the present

specification, for example, by the first full paragraph of page 8, which discloses that when a first pulse is applied to the gate line, a second pulse having an opposite polarity to the first pulse is applied to the wiring. Specifically, for example, the present specification discloses the following:

> In the above description, the signal to be applied to the second wiring is required to have the opposite polarity (opposite phase) to the gate pulse. This does not means only that if the gate pulse is positive, the second signal is negative. That is, the pulse height of an optimum signal to be applied to the second wiring is the sum of the potential of the second wiring at the non-selection time and the potential of $-C_1V_1/C_2$. That is, the opposite polarity of this invention means that the potential of the signal to be applied to the second wiring is shifted (varied) in the opposite direction to the shift (variation) direction of the potential of the gate pulse. Accordingly, for example, when the potentials of the gate at the non-selection time and the second wiring are set to 0V and 10V and the potential of the gate line at a selection time is set to 8V, the potential of the second wiring is required to be below 10V, however, it is not necessarily required to be negative.

New independent claim 54 further limits claim 53 regarding the timing of the first and second pulses. This feature is supported in the present specification, for example, by the second full paragraph of page 5, which discloses the timing of the first and second pulses. Specifically, for example, the present specification discloses the following:

> According to further consideration of the inventor, the following matter has been also found. If, irrespective of the complete synchronization between the gate pulse and the pulse of the second wiring, the device is so designed that the pulse of the second wiring is intermitted (dropped or cut) after the gate pulse is intermitted (dropped or cut), the same effect as obtained when the gate pulse and the second-wiring pulse are completely synchronized with each other would be obtained although the potential of the picture-element electrode is temporally varied. The pulse starting time for the gate pulse may be earlier or later than that of the second-wiring pulse because ΔV occurs at the off-time of the gate pulse.

New independent claims 55-60 recite various combinations of the above referenced features.

New independent claims 61-72 are similar to claims 55-60 but the specific feature of a thin film transistor is omitted in claims 61-72.

New independent claims 73-77 are similar to claims 52, 54, 56 and 59 but the specific features of an insulating flattening film and a pixel electrode being transparent are omitted in claims 73-77.

New independent claims 78-80 are supported in the present specification, for example, by Figure 1(B), in that a pixel electrode overlaps a second gate line to form a capacitor.

New independent claims 81-83 are also supported in the present specification, for example, by Figure 1(B).

For the reasons stated above and already of record, the Applicant respectfully submits that new claims 50-120 are in condition for allowance.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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